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Lanthanoid Implantation for Effective Work Function Control in NMOS High-κ / Metal Gate Stacks

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Abstract. Effective work function instability of high-κ / metal gate MOS stacks after high temperature treatment results in device threshold voltage shifts and is one of the problems associated with the gate-first integration of high-κ dielectrics in the CMOS process flow. The exact reason for this instability is subject of intense debate. In this paper it is shown that a positive threshold voltage shift due to thermal treatment can be compensated by implanting the lanthanoids lanthanum or dysprosium into the high-κ stack.

Keywords: ion implantation, lanthanoids, nmos, high-κ, work function
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INTRODUCTION

Positive and negative shifts in the effective work function (EWF) for NMOS and PMOS devices, respectively, after S/D anneal (≈ 900 – 1000°C) are a major hurdle for the gate-first integration scheme of high-κ / metal gate (HKMG) stacks [1]. This could be addressed by applying a gate-last integration scheme, where the metal gate electrodes are deposited after S/D annealing [2]. The gate-first approach is, however, less complex, since fewer masks and process steps are required. Several methods, such as lanthanum-based [3, 4] and aluminum-based [5] capping layers have been proposed as solutions to the challenges of the gate-first integration scheme.

In this paper, however, a less complex way of incorporating the required additional elements is pursued: ion implantation is an outstanding method in order to precisely introduce a well defined amount of dopants into the gate stack. This paper discusses the decrease of the EWF due to lanthanoid implantation in order to reduce the threshold voltage of NMOS devices. In previous experiments, it was shown that La and Dy implantations reduce the threshold voltages of poly / SiO_2 stacks significantly [6]. The obtained shifts increased with the lanthanoid concentration in the oxide. La implantations led to shifts of up to -3 V and were, therefore, more effective than Dy implantations, where shifts of up to -2 V were realized. Variations of implantation doses and energies, however, showed significantly smaller shift variations for La doping, indicating a lower susceptibility to fluctuations of layer thicknesses. The main focus in this paper, therefore, is set on La implantations into gate stacks with a high-κ dielectric, the latter being mainly $HfSiO_x$ but also HfO_2. In addition, results for Dy implantations are shown and compared with those of the La implantations.

EXPERIMENTAL

Ion implantation of lanthanoids

Since no gaseous source feed materials exist for the implantation of lanthanoids, a high temperature ion source has to be used in order to evaporate either the pure lanthanoids or appropriate compounds. For many lanthanoids, such as La or Dy, it is recommended to use halides or oxides, such as $LaCl_3$ or La_2O_3 for La implantation, others, such as Yb, can be evaporated directly from elemental status [7]. For the La and Dy implantations in this work, $LaCl_3$ and $DyCl_3$, respectively, were used.

In order to limit both, La doping of the Si substrate and defect generation in the dielectric, the implantation profiles were tailored so that the projected range laid in the metal layer while the doping of the high-κ layer was realized by the profile's tail. This requires an appropriate choice of the metal thickness and the implantation energy, considering that the latter cannot be chosen arbitrarily low in order to obtain a sufficient ion current. This is illustrated in Fig. 1, where a SRIM simulation of a La implantation with an energy of 30 keV into a TiN (40 nm) / HfO_2 (8 nm) / SiO_2 (20 nm) stack is shown. When the HfO_2 layer is exchanged with $HfSiO_x$, the simulated La profile remains nearly the same. The implanted La is expected to diffuse into the dielectric during high temperature annealing.

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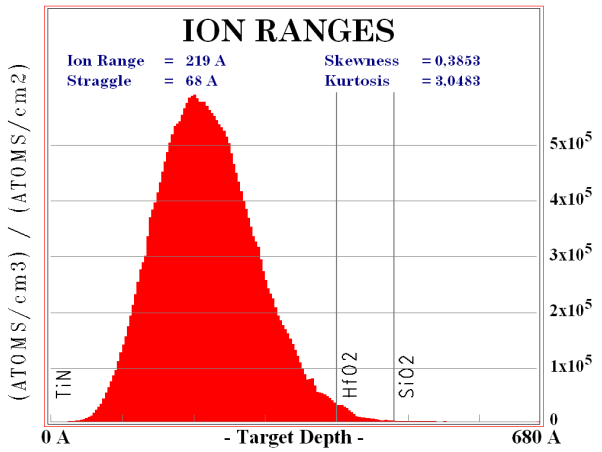

FIGURE 1. SRIM [8] simulation of the La distribution in the TiN (40 nm) / HfO_2 (10 nm) / SiO_2 (20 nm) gate stack. Energy of La implantation: 30 keV.

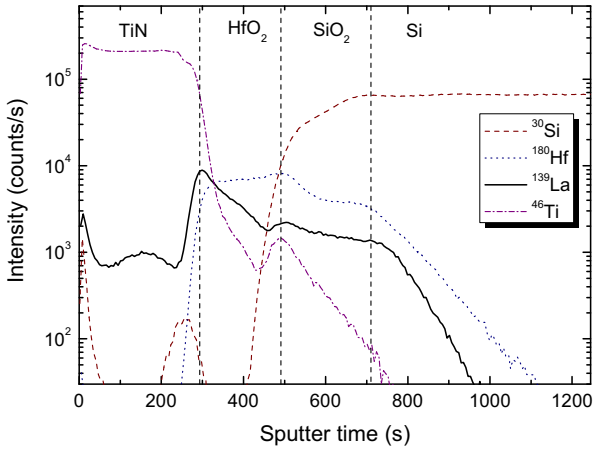

FIGURE 2. SIMS measurements of La, Ti, Hf, and Si in a TiN / HfO_2 / SiO_2 stack. Implantation parameters: La, 30 keV, $5{\cdot}10^{14}$ cm^{-2}. Annealing: 900°C, 20 s, followed by 1070°C, 5 s

Sample preparation

MOS capacitor stacks of TiN (40 nm) / $HfSiO_x$ (10 nm) / SiO_2 (1 nm) and TiN (40 nm) / HfO_2 (8 nm) / SiO_2 (1 nm) were fabricated on silicon wafers with SiO_2 field isolation. Further, stacks with the same layer sequence and an SiO_2 thickness of 20 nm were fabricated in order to evaluate the influence of the oxide on the EWF and for SIMS measurements. Part of the samples was implanted with either La or Dy at energies of 30 or 50 keV, respectively, and a dose of $5{\cdot}10^{14}$ cm^{-2}. After implantation, the samples underwent a high temperature anneal under S/D conditions of 900°C for 20 s, followed by 1070°C for 5 s. The samples were characterized by SIMS, capacitance-voltage (CV) and gate leakage current measurements.

RESULTS

Profile measurements

Profiles of the La distribution as well as the gate stack elements of the annealed stack were analyzed by SIMS with a Cameca WF. Since the sputter rates of the layers and the ionization rates of the measured elements in the layers were not known, the measurements have to be interpreted qualitatively. Figure 2 shows the measured intensity of the elements La, Ti, Hf, and Si as a function of sputter time. In the middle of the TiN layer, the implanted La profile is visible which correlates well with the simulation in Fig. 1. The reason why the La intensities in the HfO_2 and the SiO_2 are higher than the La intensities in the TiN is attributed to the presence of oxygen in the dielectric layers, therefore, the ionization rates are much higher than in TiN. Despite of the different ionization energies, the measurement clearly indicates that due to the annealing step a considerable amount of La diffuses into the gate stack. In the HfO_2 the La concentration falls towards the SiO_2, where the La concentration is more or less constant. At the SiO_2/Si interface towards the silicon, the La concentration tapers off. Since such tails are well-known SIMS artifacts, it might be speculated that no La was introduced into the Si substrate.

CV measurements

Figure 3 compares the C-V curves for La-doped (30 keV, $5{\cdot}10^{14}$ cm^{-2}) and non-implanted TiN / $HfSiO_x$ / SiO_2 stacks. Thereby, the La implantation causes a shift of about -0.5 V which corresponds to a reduction of the EWF from 4.4 eV to 3.9 eV for the device. This shift is, on the one hand, significantly lower than the shifts obtained in case of a SiO_2 dielectric [6]; on the other hand, an EWF of 3.9 eV comes very close to the work function of n-doped poly silicon of about 4.0 eV.

A similar EWF value of 3.8 eV was reached for Dy implantation (50 keV, $5{\cdot}10^{14}$ cm^{-2}). With SRIM, a projected range of 28 nm was simulated for Dy in TiN which is significantly larger than the 22 nm for La (cf. Fig. 1). In order to achieve the same shift in EWF, the concentration of Dy in the dielectric has to be, therefore, significantly larger than that of La.

To get a better understanding of the discrepancy of the EWF shifts between high-κ dielectrics and SiO_2, further Dy implanted stacks were characterized. The layer se-

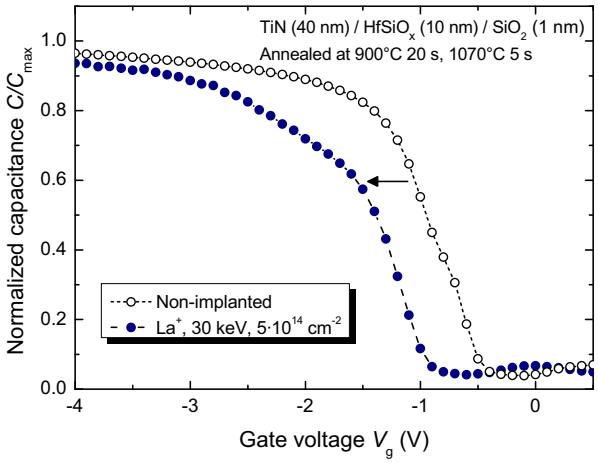

FIGURE 3. Comparison of the C-V characteristics of La doped and non-doped TiN / $HfSiO_x$ / SiO_2 gate stacks. Implantation parameters: La, 30 keV, $5{\cdot}10^{14}$ cm^{-2}

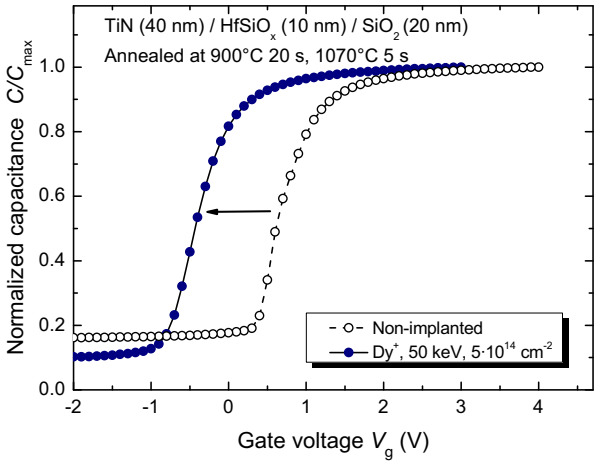

FIGURE 4. Comparison of the C-V characteristics of Dy doped and non-doped TiN / $HfSiO_x$ / SiO_2 gate stacks. Implantation parameters: Dy, 50 keV, $5{\cdot}10^{14}$ cm^{-2}

quence of the stacks was the same as above, only the thickness of the SiO_2 was increased to 20 nm and the Si substrate was changed to n-type material. As Fig. 4 shows, the Dy implantation (50 keV, $5{\cdot}10^{14}$ cm^{-2}) produced a shift of about -1 V, which is significantly larger than the shift of the Dy implanted device with 1 nm SiO_2 and the La implanted device (3). The larger shift can be, therefore, attributed to the thicker SiO_2 layer. Thus, penetration of Dy into the SiO_2 layer may account for the stronger shift observed with the thicker SiO_2 layer.

First La implantations (30 keV, $5{\cdot}10^{14}$ cm^{-2}) were also performed in stacks with HfO_2 instead of $HfSiO_x$. It turned out that the shift is, with approx. 0.7 V, slightly larger than for the stacks with $HfSiO_x$. This indicates that

TABLE 1. Obtained EWF shifts ΔEWF for La and Dy implantations in TiN (40 nm) / dielectric stacks.

Dielectric (Thickness (nm))	Ion	Energy (keV)	Dose (cm^{-2})	ΔEWF (eV)
$HfSiO_x$ (10) / SiO_2 (1)	La^+	30	$5{\cdot}10^{14}$	0.5
$HfSiO_x$ (10) / SiO_2 (1)	Dy^+	50	$5{\cdot}10^{14}$	0.6
$HfSiO_x$ (10) / SiO_2 (20)	Dy^+	50	$5{\cdot}10^{14}$	1.0
HfO_2 (8) / SiO_2 (1)	La^+	30	$5{\cdot}10^{14}$	0.7

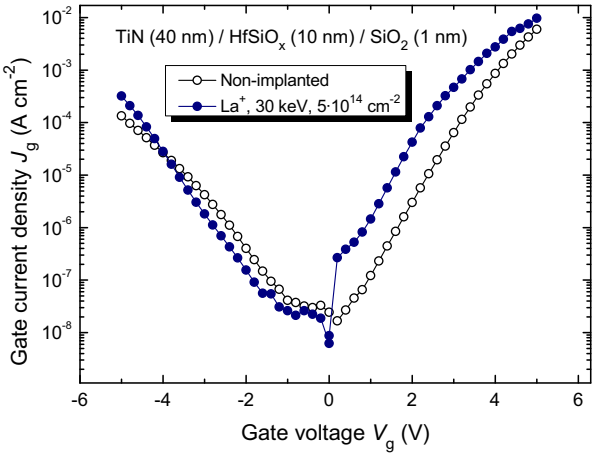

FIGURE 5. Comparison of the gate leakage current densities of La doped and non-doped TiN / $HfSiO_x$ / SiO_2 gate stacks. Implantation parameters: La, 30 keV, $5{\cdot}10^{14}$ cm^{-2}

implantation energy and dose may be reduced in order to get shifts of about 0.5 to 0.6 V.

A summary of the obtained EWF shifts for the experiments is given in Tab. 1.

Gate leakage measurements

Figure 5 compares the gate leakage currents for non-implanted devices and La implanted MOS devices. For negative gate voltages, the gate current density for implanted and non-implanted devices are about the same. For positive gate voltages, however, the leakage current for the implanted device is about one order of magnitude larger than for the non-implanted device. This might be attributed to radiation damage to the dielectric, causing a lowering of the barrier at the SiO_2 / Si interface. Possibly, the gate leakage current might be reduced by minimizing the damage to the dielectric stack, thus, by reducing implantation energies.

DISCUSSION

The threshold voltage shift is attributed to charge generation in the dielectric after annealing, resulting from oxygen out-diffusion from the high-κ to the silicon interface to form SiO_2 [9, 10]. The compensating effect of the lanthanoids can also be attributed to the generation of compensatory positive charge in the high-κ dielectric, which compensates the negative oxide charge generated during the formation of oxygen vacancies [11].

The direction of the V_{fb} shift in high-k based devices after annealing depends on the position of the Fermi level [1, 9]. For PMOS devices, a negative flat-band voltage shift is observed while for NMOS devices, a positive shift is observed. In our results here, La was implanted in a p-type substrate while Dy was also implanted in an n-type substrate. A negative shift in the C-V characteristic is observed for both implanted elements and both substrate types. This indicates that the direction of shift on doping with the lanthanoids is independent of the doping in the silicon substrate.

CONCLUSION

The implantation of both elements, La as well as Dy, into metal / high-κ gate stacks leads to a decrease of the EWF of the stack. For Dy, however, a higher concentration in the dielectric is required to produce the same shift of the EWF as La. This favors La as first choice, since the radiation damage in the dielectric is smaller than for Dy. Concerning dielectric layers, the implantation of La was successfully applied on gate stacks containing $HfSiO_x$ or HfO_2 layers. For the same implantation conditions, the EWF shift for HfO_2 was more distinctive than for $HfSiO_x$. The shift of the EWF in the used high-κ stacks is less pronounced than for oxides, but the obtained EWF shifts of 0.5 to 0.7 V are sufficient in order to compensate the shifts caused by high temperature annealing. The impact of thickness fluctuations of the metal layer on the EWF shift have not yet been considered. Results for poly/ SiO_2 stacks, however, indicate that EWF fluctuations might be smaller for La doping rather than for Dy. The leakage currents for La implanted stacks are up to one order of magnitude larger than for the non-implanted stack. Possibly, the leakage currents can be reduced by optimization of the implantation parameters (e. g., slightly reducing the energy).

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